**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Previously presented): A wafer level package comprising:

a semiconductor wafer having at least one semiconductor chip circuit forming region each including a semiconductor chip circuit and a plurality of chip terminals, said chip terminals including at least one test chip terminal and at least one non-test chip terminal;

at least one external connection terminal electrically connected to said at least one non-test chip terminal;

at least one redistribution trace provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out of said semiconductor chip circuit forming region to a position offset from said one of said test chip terminals;

at least one testing member provided in an outer region of said semiconductor chip circuit forming region of said semiconductor wafer, said second end of said redistribution trace being connected to said at least one testing member;

an insulating material covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material, and

a sealing resin provided on said insulating material such that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin.

2. (Canceled)

3. (Original): The wafer-level package as claimed in claim 1, wherein said at least one external connection terminal and said at least one non-test terminal are electrically connected by an internal redistribution trace in such a manner that said at least one external connection terminal is provided at a position within said semiconductor chip circuit forming region and offset from said at least one non-test chip terminal.

4-20. (Canceled)